**Motivation**

- We propose an aging Resilient RO PUF design for FPGA exploiting the SRAM cells and multiple paths available in FPGA LUTs.
- Advantages of presented PUF:
  - Average improvement of 37% in aging degradation compared to conventional RO PUF.
  - Average improvement of 37.4% on reliability compared to conventional RO PUF.

**Theory and Background**

- Aging in transistors and their types
  - Results from trapped charges and broken bonds at gate dielectric interfaces which increases \( V_{th} \) in scaled monodevices.
  - Bias Temperature Instability (BTI)
    - Results in a positive shift in the absolute value of \( V_{th} \).
  - BTI Recovery occurs when: \( |V_{gs}| = 0, |V_{ds}| = V_{dd} \)

- Hot Carrier Injection (HCI)
  - During switching, the accelerated carriers drift towards drain under the influence of the lateral electric field generating secondary carriers through impact ionization.
  - HCI occurs when \( |V_{gs}| = V_{dd}, |V_{ds}| = V_{dd} \)

- Increases \( V_{th} \) and decreases switching speed. It is negligible for higher technology nodes but increases for technology nodes <40nm.

- LUT structure and LUT based RO in FPGA
  - Popular LUT structure in FPGA include Pass transistor structure and T-gate structure.

**Simulation Results**

- A set of 50 RO PUF instances are simulated in Hspice using Monte Carlo and MOSRA aging degradation tool.
  - PTM 90 nm model card is used as the technology node.
  - In Hspice, the ROs are modeled using LUT based FPGA architecture as shown before.

- Both LUT structures are simulated with every RO PUF consisting of 128 ROs generating a 64-bit response.
  - The comparison time is 10µs and the ROs are aged using MOSRA tool for an accelerated aging for 1 year.

**Experimental Setup and Measurement**

- Silicon measurement results are calculated with Elbert Spartan 3A FPGA boards (90nm tech node).
  - A set of five Elbert V2 boards are programmed with conventional RO PUF design with 110 ROs laid out.
  - Initial frequency data is taken at normal supply voltage (1.25V) and room temperature 27°C.
  - The boards are aged at 1.45V supply voltage and 100°C temperature using Tempronix Thermostream.
  - Post aging frequency data is collected.

**Conclusion**

- The steps mentioned before are repeated for five FPGAs with proposed RO PUF and results are
  - Silicon results show an average improvement of 37% in aging degradation of proposed RO PUF.

- The Reliability of the proposed PUF is improved by 37.4%.

- Sleep path and oscillation indicates similar aging which hints the LUT architecture is PT based.

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